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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,223	07/29/2003	Om P. Agrawal	M-15169US	5335

7590 07/13/2004

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,223	AGRAWAL ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 9-11, 17-18, 20, and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by North U.S. Patent No. (6,622,208).

In reference to claim 1, North discloses in Figure 9 a clock generator comprising: a first circuit (906a) adapted to programmably receive an input signal, having a possible range of voltage levels and signal types, and modify a frequency of the input signal by a first programmable amount (M1) to generate a first input signal; a feedback loop circuit (/N1) adapted to receive a feedback signal and modify a frequency of the feedback signal by a second programmable amount (N1) to generate a second input signal; a phase-locked loop circuit (121a) adapted to receive the first input signal and the second input signal and provide a first output signal (VCOCLK1); and a second circuit (903a-c) adapted to receive the first output signal to generate a plurality of second output signals having programmable frequencies, wherein the first and second programmable amount and the programmable frequencies are determined by data stored in electrically erasable memory (122, see figure 1). The same applies to claims 17-18 and 26-29.

In reference to claim 2, North discloses in column 12, lines 9-10 input/output boundary scan circuits adapted to provide JTAG test support for the clock generator. The same applies to claims 3, and 20.

In reference to claim 9, the signal types in North may comprise single-ended and differential signals.

In reference to claim 10, North discloses in Figure 9 a plurality of output circuits (904 and the circuit receiving UARTCLK1) and programmably provide a plurality of third output signals having a range of selectable voltage levels, signal types, and output impedance. The same applies to claim 11.

3. Claims 21, 23, 25-26, and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Moore U.S. Patent No. (6,690,224).

In reference to claim 21, Moore discloses in Figure 3 a clock generator comprising: a an input circuit (receiving signal REFCLK(N)) programmable to receive input signals of various signal types and voltage levels and to generate in response an input signal to a phase-locked loop (200); a phase-locked loop circuit (200) adapted to receive the PLL input signal and to generate in response a PLL output signal (214a-214n, FB); and an output circuit (208, 210, 212) adapted to receive the PLL output signal and be programmable to generate in response clock signals of various signal types and voltage levels. The same applies to claims 26 and 28.

In reference to claim 23, Moore discloses in Figure 3 a clock divider circuit (206a-206n) coupled between the phase-locked loop and the output circuit and programmable to modify a frequency of the PLL output signal.

In reference to claim 25, Moore discloses in Figure 3 input/output boundary scan circuits (211) adapted to provide JTAG test support for the clock generator.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-30 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-2, 5-12, 14-19, 21-24, and 26-30 of copending Application No. 10/629221. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: an input circuit, a feedback loop circuit, a phase-locked loop circuit a divider circuit, and an output circuit.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other

copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Allowable Subject Matter

6. Claims 13-16 are allowed.

7. The following is an examiner's statement of reasons for allowance: Claims 13-16 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit comprises means for selecting from a plurality of input signals (210); means for selecting from a plurality of feedback signals (212, 214) and means for providing configurability and in-system programmability (110, see Figure 1) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-

1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

July 9, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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